UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,168	08/05/2003	Eun-Ae Chung	5649-1138	6337

20792 7590 12/14/2004

MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
LUHRS, MICHAEL K	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,168	CHUNG ET AL.	
	Examiner	Art Unit	
	Michael K. Luhrs	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01 July 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-15, drawn to method, classified in class 438, subclass 586.

II. Claims 16-20, drawn to device, classified in class 257, subclass 44.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process, such as forming the ILD after exposing the silicon to delta-dopant.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Attorney O'Sullivan on 11/22/04 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-15. Affirmation of this election must be made by applicant in replying to this Office action. Claims 16-20 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Objections

6. Claims 11-13 are objected to because of the following informalities: There are no additional method steps in claims 11-13. Device claims are *not* limited to the recited process (MPEP 2113). Regarding claim 11, should the applicant intend that *the silicon based region* be *doped with the first impurity type*, then the applicant should recite the method steps to do so. Regarding claim 12, should the applicant intend that *the silicon based region* comprise a *contact plug*, then the applicant should recite the method steps to do so. Regarding claim 13, should the applicant

intend that *the silicon based region* comprise a *polysilicon contact plug doped with the first impurity type*, then the applicant should recite the method steps to do so. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-7, 11 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakano USPN 5,183,781.

Regarding claim 1, Nakano teaches: *a method of fabricating a contact of a semiconductor device, comprising: patterning an interlayer dielectric of the semiconductor device to form a contact hole that exposes a silicon-based region of a first impurity type;* as ILD layer 103 (line 62, column) exposes doped region 102 (line 56, column 3), *doping the exposed silicon-based region with a gas containing an element of the first impurity type;* as phosphorus impurity (line 67-68, column 3) *and forming a contact plug in the contact hole,* as the doped polysilicon layer 105 (lines 3-4, column 4) all as shown in Fig. 1d.

Regarding claim 2, Nakano teaches: *the method of Claim 1, wherein the first impurity type is an n-type*, since in the example, region 102 is n-type diffusion layer (in line 56, column 3).

Regarding claim 3, Nakano teaches: *the method of Claim 1, wherein the gas containing an element of the first impurity type comprises AsH_3 and/or PH_3*, because PH_3, is used in line 34, column 4 and line 53, column 5.

Regarding claim 4, Nakano teaches: *the method of Claim 1, wherein the contact plug comprises doped polysilicon,* because the doped polysilicon layer 105 (lines 3-4, column 4) *is* the plug used to form the electrical connection from the diffusion layer in the semiconductor substrate (lines 44-46, column 6).

Regarding claim 5, Nakano teaches: *the method of Claim 4, wherein the doped polysilicon is doped with an element of the first impurity type*, because in the example the diffusion layer in the substrate is n-type (line 56, column 3) and the doped polysilicon can be phosphorus (line 67, column 3) or arsenic or boron (lines 7-8, column 5), hence the *doped polysilicon*, doped with an n-type dopant disclosed would match the diffusion region n-type dopant in the example, is therefore considered as doped polysilicon doped with an element of the first impurity type.

Regarding claim 6, Nakano teaches: *the method of Claim 5, wherein the element of the first impurity type comprises phosphorus and/or arsenic,*. because in the example the diffusion layer in the substrate is n-type (line 56, column 3) and the doped polysilicon can be phosphorus (line 67, column 3) is therefore *phosphorus*.

Regarding claim 7, Nakano teaches: *the method of Claim 1, wherein doping the exposed silicon-based region with a gas containing an element of the first impurity type and forming a contact plug in the contact hole are performed in a chamber of the same manufacturing apparatus in-situ*, since the polysilicon layer 105 is grown while supplying the phosphorus (lines 67-68, column 3).

Regarding claim 11, Nakano teaches: *the method of Claim 1, wherein the silicon-based region comprises a region of a silicon substrate doped with the first impurity type*, because, in fact the given *p-type substrate* is silicon (line 54, column 3), and that has a diffusion layer 102 of n-type (line 56, column 3), inherently, the substrate must have been doped, for the layer 102 to be expressed as it is i.e. a *diffusion* layer. This is given, i.e. the diffusion layer 102 is representative of a source or drain of a MOS transistor (lines 56-57, column 3) such layers to be called diffusion layers are recognized as having been doped.

Regarding claim 14, Nakano teaches: *the method of Claim 1, further comprising: forming a diffusion layer of the first impurity type in a semiconductor substrate of a second impurity type; depositing an interlayer dielectric on a surface of the semiconductor substrate where the diffusion layer of the first impurity type is formed; and wherein patterning an interlayer dielectric of the semiconductor device to form a contact hole that exposes a silicon-based region of a first impurity type comprises patterning the interlayer dielectric to form a contact hole that exposes the diffusion layer of the first impurity type as the exposed silicon-based region,* because, in fact the given *p-type substrate* is silicon (line 54, column 3), and that has a diffusion layer 102 of n-type (line 56, column 3), inherently, the substrate must have been doped, for the layer 102 to be expressed as it is, i.e. a *diffusion* layer. This is given, i.e. the diffusion layer 102 is representative of a source or drain of a MOS transistor (lines 56-57, column 3) such layers to be called diffusion layers are recognized as having been doped. Therefore a p-type substrate is a semiconductor substrate of a second impurity type, namely the p-type, whereas the diffusion layer is the first impurity type, namely the n-type. The ILD (layer 103 in Fig. 1d) is clearly patterned to have the opening shown to the diffusion layer (102).

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-3, 8, 11, 12, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Sharan et. al. USPN 6,642,620 (hereinafter as "Sharan").

Regarding claim 1, Sharan teaches: *a method of fabricating a contact of a semiconductor device, comprising: patterning an interlayer dielectric of the semiconductor device to form a contact hole that exposes a silicon-based region of a first impurity type;* see patterning, line 40, column 1, as insulating layer 14 on semiconductor structure 10, Fig. 1 (lines 59-66, column 2), *doping the exposed silicon-based region with a gas containing an element of the first impurity type*; the contact area 12 is comprised of doped, (hence a first impurity type), semiconductor material (lines 1-2, column 3), the opening formed thereto (line 67, column 2) by anisotropic etch (line 3-4, column 3) and then exposed to the plasma gas (lines 42-55, column 3), whereas the gas can be dopant gas (lines 56-59, column 3) *and forming a contact plug in the contact hole,* a contact layer formed, such as contact 40, shown in Fig. 7 (lines 23-24, column 4).

Regarding claim 2, Sharan teaches: *the method of Claim 1, wherein the first impurity type is an n-type,* the dopant can be *any* dopant type (line 59-60, column 3) but the preferred dopant is the same dopant that is in the doped semiconductor (lines 61-62, column 3) would therefore be inclusive to either n-type or p-type since both types are known to have contacts made thereto.

Regarding claim 3, Sharan teaches: *the method of Claim 1, wherein the gas containing an element of the first impurity type comprises AsH_3 and/or PH_3,* because sources of boron, phosphorus, or arsenic (listed in lines 58-60, column 4) would include these compatible sources.

Regarding claim 8, Sharan teaches: *the method of Claim 3, wherein doping the exposed silicon-based region with a gas containing an element of the first impurity type is performed at a temperature of from about 400 to about 800 °C,* since the temperature is at 650°C (lines 38-39, column 3), would therefore fall into the claimed range of 400 to 800°C is therefore about from 400 to about 800°C.

Regarding claim 11, Sharan teaches: *the method of Claim 1, wherein the silicon-based region comprises a region of a silicon substrate doped with the first impurity type,* because, it is mentioned that the dopant may be any dopant,

although the same is preferred (lines 56-63, column 3) of the doped semiconductor material, hence, whatever it may be doped with, it is considered as the first impurity type.

Regarding claim 12, Sharan teaches: *the method of Claim 1, wherein the silicon-based region comprises a contact plug,* since the "silicon based region" such as contact area '12' (line 63, column 3), has contact layer 40 (line 23, column 4) in its vicinity, as shown in Fig. 7.

Regarding claim 14, Sharan teaches: *the method of Claim 1, further comprising: forming a diffusion layer of the first impurity type in a semiconductor substrate of a second impurity type;* (the semiconductor is doped , see lines 1-2, column 3) *depositing an interlayer dielectric on a surface of the semiconductor substrate where the diffusion layer of the first impurity type is formed*; ILD layer 14, (line 65, column 2), is etched to form openings (line 3, column 3) over the contact area 12, (contact area is doped semiconductor material), lines 1-2, column 3) *and wherein patterning an interlayer dielectric of the semiconductor device to form a contact hole that exposes a silicon-based region of a first impurity type comprises patterning the interlayer dielectric to form a contact hole that exposes the diffusion layer of the first impurity type as the exposed silicon-based region,* because, the contact opening is formed (line 67, column 2) by etching is thus a patterning process, viz, it is patterned in claim 1, exposes the contact area 12 comprised of the doped semiconductor material, i.e. it is the diffusion layer of first impurity, inherently the semiconductor substrate is considered also doped to be a semiconductor, hence as a second impurity.

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharan as applied to claim 1 above, and further in view of Ho 4,898,841.

Regarding claim 4, Sharan is silent on: *the method of Claim 1, wherein the contact plug comprises doped polysilicon,* only mentioning the silicides (in lines 23-28, column 4). However a contact plug *comprising doped*

polysilicon as well known, as taught by Ho, for example for the metal (lines 47-50, column 2),whereas in the example of tungsten silicide (lines 25-26, column 5), doped polysilicon may be substituted (lines 56-57, column 5), would therefore comprise the plug with *doped polysilicon*. Ho teaches the *contact plug comprises doped polysilicon* for the purpose of providing better adherence for the metal. Since Ho and Sharan are both from the same field of endeavor, the purpose disclosed by Ho would have been recognized in the pertinent art of Sharan. It would have been obvious at the time the invention was made to a person having ordinary skill in the art that other materials could comprise the plug such as the doped polysilicon to better adhere the metallization.

Regarding claim 13, Sharan is silent on: *the method of Claim 1, wherein the silicon-based region comprises a polysilicon contact plug doped with the first impurity type*, since the plug is of a silicide. Ho teaches the silicon based region *comprises polysilicon* for the purpose of providing better adherence for the metal. Since Ho and Sharan are both from the same field of endeavor, the purpose disclosed by Ho would have been recognized in the pertinent art of Sharan. It would have been obvious at the time the invention was made to a person having ordinary skill in the art that other materials could comprise the plug such as the polysilicon to better adhere the metallization.

12. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharan as applied to claim 3 above.

Regarding claim 9, Sharan silent on: *the method of Claim 3, wherein doping the exposed silicon-based region with a gas containing an element of the first impurity type is performed under a chamber pressure of from about 6x 10^{-2} to about 6x 10^{-4} Torr,* however discloses a pressure of 1-5 Torr (line 33, column 3), and, regarding claim 10, Sharan silent on: *the method of Claim 3, wherein doping the exposed silicon-based region with a gas containing an element of the first impurity type is performed from about 30 to about 180 seconds,* yet the dopant may be separate from the plasma clean (lines 1-4, column 5) time. Therefore, regarding claims 9 and 10, one having ordinary skill in the art would have been able to, by routine experimentation, optimize the pressure and time for a desired dopant profile. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to optimize the chamber pressure and dopant exposure time in order to achieve the desired dopant profile. The particular parameters of pressure and time (claims 9 and 10 respectively) are obvious result-effective variables, i.e., variables which achieve a recognized result (i.e. the amount of time the dopant is supplied with a particular chamber pressure

would yield a particular profile), hence workable ranges of said variables might be characterized as routine experimentation. MPEP 2144.05 [R-1] , II, B.

13. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano as applied to claim 1 above, in view of Park et. al. USPN 6,509,263.

Regarding claim 15, Nakano teaches: *the method of Claim 1, further comprising: forming a diffusion layer of the first impurity type in a semiconductor substrate of a second impurity type;* (i.e. p-type substrate, n-type diffusion region (lines 54 and 56, column 3), hence the p-type is second impurity) *depositing a first interlayer dielectric on a surface of the semiconductor substrate where the diffusion layer of the first impurity type is formed;* (the ILD 103 is already 'patterned' in claim 1 hence it must have been deposited, notwithstanding, see line 63, column 3, i.e. deposited by CVD) and selective etching to form opening: *forming a first contact hole in the first interlayer dielectric* (already performed in claim 1) *to expose the diffusion layer of the first impurity type;* (i.e. it in fact does expose the n-type diffusion region 102, see Fig. 1a) *forming a first contact plug in the first contact hole using a doped polysilicon;* doped polysilicon 105 in Fig. 1b, line 67, column 3. Nakano is silent on the second interlayer thus is silent regarding: *depositing a second interlayer dielectric on a surface of the semiconductor substrate where the first contact plug is formed; wherein patterning an interlayer dielectric of the semiconductor device to form a contact hole that exposes a silicon-based region of a first impurity type comprises patterning the second interlayer dielectric to form a second contact hole that exposes the first contact plug as the exposed silicon-based region.* Park et. al. deposits a second ILD (uses photoresist to pattern) line 16, column 4, and also subjects the plug to a treatment of PH_3 to reduce contact resistance, see Fig. 3d, (lines 23-26, column 4). Since Park et. al. and Nakano are both from the same field of endeavor, the purpose disclosed by Park et. al. would have been recognized in the pertinent art of Nakano. It would have been obvious at the time the invention was made to a person having ordinary skill in the art that additional ILD may be formed for higher metallization and connections with good contact to the first plug.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Chang et. al. USPN 4,516,145 teach an inert treatment to restore dopant to the exposed semiconductor. Cunningham et. al. USPN 4,780,748 teach a delta-doped ohmic contact. Ogino USPN 5,188,987 teaches n+doped regions 6s and 6d on n-doped source drain regions 2s and 2d in Fig. 1D; Ogino teaches that prior art has the SEG layer 46 with *single*

crystal silicon and polycrystalline layer 44, (column 1) whereas in Ogino's improvement does not clearly specify whether silicon layers 6s and 6d are single crystal or not, see line 26-27, column 4. Drowley et. al. USPN 5,310,711 teach dilute dopant gas for forming shallow junctions. Aisou USPN 6,074,925 teaches a sequence of LPCVD polycrystalline followed by tungsten silicide and an amorphous silicon containing phosphorus thereover,layers 12, 13, 14, respectively, lines 44-55, column 4), shown in Fig. 3B. Oda USPN 6,162,668 teaches embodiment 5, line 23-25, with epitaxial layer 8a containing impurities and metallic wiring layer 9, Fig. 21,, to relax the electric field, see lines 39-41, column 9). Ota et. al. USPN 6,274,889 teach the ohmic electrode for SiC semiconductor substrate . O'Toole et. al. USPN 6,492,192 teach contact to Schottky diode, i.e. tungsten then metal. Citrin et. al. USPN 6,403,454 teach delta doping (various locations: under or over S/D regions, see lines 41-46, column 3). Cheong et. al. USPN 6,521,508 teach in situ doping of SEG (selective epitaxial growth) contact plug into USG. Oikawa et. al. USPN 6,627,473 teach delta doped layer under the etch stop layer. Yokogawa et. al. USPN 6,674,131 teach multilayer of delta doped and undoped regions. Cheong USPN 6,818,537 teach adding the GeH4 dopant to the already doped PH3 silicon for better selectivity and speed to the PE-USG.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael K. Luhrs whose telephone number is 571-272-1874. The examiner can normally be reached on M-F, 8-5.

16. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

17. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael K. Luhrs
12/08/04

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800